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| (84) Designated Contracting States:<br>AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC<br>NL PT SE<br>Designated Extension States:<br>AL LT LV RO SI | (71) Applicant:<br>STMicroelectronics S.r.l.<br>20041 Agrate Brianza (Milano) (IT)<br>(72) Inventor: Baldi, Livio<br>20041 Agrate Brianza (Milano) (IT) |
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(54) Currency note comprising an integrated circuit

(57) The present invention relates to a currency note (BN) provided with an identification and/or authentication element consisting of an integrated circuit (IC) which can store, securely in electronic form, accessible from outside, such information as: the value, serial number, issuer, and date of issuance.

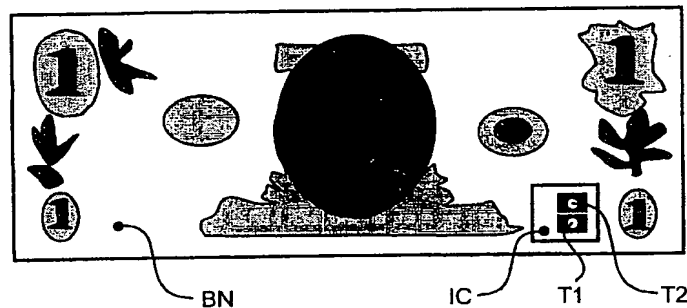


Fig.9

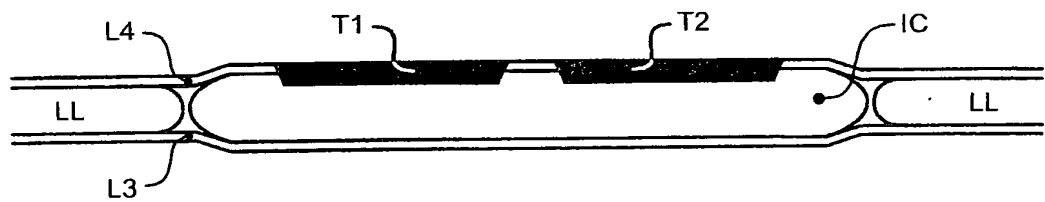


Fig.10

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## Description

[0001] This invention relates to currency notes incorporating an identification and/or authentication element.

[0002] The identification and authentication of currency notes, such as banknotes, checks, stocks, and bonds, is a long-standing problem.

[0003] Reference will be made hereinafter to banknotes, although the invention is not limited thereto.

[0004] Little has been achieved in the direction of banknote identification, besides the overprinting of serial numbers. Invisible paint markings have been used occasionally for ransom payments.

[0005] On the other hand, much has been done to have banknotes authenticated, in an effort to defeat an alert counterfeiting industry.

[0006] Among the techniques adopted are: the use of special papers, special inks and special patterns, the inclusion of watermarks and the inclusion of plastics, metal or magnetic strips. Some of these techniques are described in US Patents 4,462,866; 4,652,015; 4,943,093; and 5,161,829, incorporated hereto by reference.

[0007] All these techniques have the disadvantage of being either easily forged or difficult to authenticate by the general public and by bank personnel.

[0008] It is the object of this invention to provide a currency note which is more secure and easy to identify and/or authenticate.

[0009] This object is achieved by a currency note having the characterizing features set forth in Claim 1. Further advantageous aspects of this invention are set forth in the subclaims.

[0010] The idea behind this invention is one of using, as an identifying and/or authenticating element, an integrated circuit applied to or embedded in the note.

[0011] The invention can be more clearly understood by reading the following description in conjunction with the accompanying drawings, where:

Figures 1, 2 and 3 respectively show three different banknotes according to the invention;

Figures 4, 5, 6, 7 and 8 show respective cross-sectional views taken through five different banknotes according to the invention at the location of the integrated circuit;

Figure 9 shows a fourth banknote according to the invention; and

Figure 10 is a vertical cross-section view taken through the banknote of Figure 9 at the location of the integrated circuit.

[0012] The use of integrated circuits applied on a substrate, such as an adhesive label, for the purpose of identifying objects, e.g. articles in a supermarket, is

known under the trademark "Supertag", and described in US Patent 5,566,441. US Patent 5,537,105 describes, on the other hand, a corresponding RFID (Radio Frequency Identification) system. This system comprises an interrogator and a plurality of passive transponders equipped with an antenna and having the integrated circuit for their electrical core piece. US Patents 5,537,105 and 5,566,441 are incorporated hereto by reference.

[0013] The utilization of integrated circuits for identifying (bank, telephone, etc.) credit accounts and their owners is known from the use of smart cards. Early smart cards had contacts, but contact-less cards have been introduced more recently. Extensive technical and patent literature is available covering the electronic, chemical and mechanical aspects of such cards.

[0014] However, integrated circuits have never been used for the purpose of identifying or authenticating currency notes, as provided by this invention, nor have the implications of such been heeded heretofore.

[0015] Figures 1, 2 and 3 show three different embodiments of a banknote BN according to the invention, which banknote incorporates an integrated circuit IC as its identifying and/or authenticating element. Alternatively, two or more integrated circuits could be interconnected within each banknote, although this choice would be less advantageous due to the difficulty of establishing a large number of electric connections within a banknote.

[0016] The integrated circuit IC is to store information that can be read by a suitable authentication apparatus external of the banknote BN, in a similar manner to the aforementioned "Supertag" system and contact or contact-less smart cards.

[0017] The items of information stored by the integrated circuit may be, for example, a real or par value, identity, date of issuance, and issuer of the note. This information may also appear in print on the note, more or less as in current practice. Based on such information, the note can be readily identified, even in an automatic manner.

[0018] In addition, the very presence of an integrated circuit capable of transmitting predetermined response signals in response to predetermined interrogation signals represents an effective authentication element. In fact, integrated circuits are no articles that can be fabricated at tyro level, and surely not at a low cost.

[0019] If required, however, measures can be taken to discourage too easy a replication of the integrated circuit, and some such measures have already been proposed and/or adopted for smart cards.

[0020] In the embodiment of Figure 3, the integrated circuit IC has no terminals, and includes an integrated antenna ANT, which may be a loop of a conductive material formed in the peripheral region of the integrated circuit. The word "terminals" means here areas of the integrated circuit which are prearranged for electrically connecting the integrated circuit to external elec-

tric and/or electronic circuits.

[0021] In this case, the interrogation and response signals are RF signals, and accordingly, the integrated circuit IC is to include suitable circuitry for receiving and transmitting them, and capable of self-feeding by RF power, similar to the integrated circuits of contact-less smart cards.

[0022] In the embodiments of Figures 1, 2 and 9, the integrated circuit IC has two terminals T1 and T2, omitted from Figures 1 and 2. These terminals may be provided on one face or on opposite faces of the integrated circuit IC.

[0023] Two terminals are a minimum for establishing between two electric systems a bi-directional transmission of informational signals and a one-way transmission of power. Of course, the integrated circuit IC may be provided with plural terminals; in general, this would bring about a simplification in the circuitry within the integrated circuit IC, but also a complication in the construction of the banknote BN.

[0024] In the embodiments of Figures 1 and 2, the banknote BN also includes an antenna which is connected to the terminals T1 and T2. Of course, the integrated circuit IC and/or the banknote BN could be provided with a receiving antenna and a transmitting antenna, although this would involve added complexity and cost.

[0025] In the embodiment of Figure 1, the antenna comprises two electric conductors C1 and C2 connected to the terminals T1 and T2, respectively, and embedded in the note. Accordingly, the antenna is an open dipole. This is similar to the arrangement provided in the "Supertag" system.

[0026] In the embodiment of Figure 2, the antenna consists of a loop LP formed from an electric conductor which has its two ends connected to the terminals T1 and T2 and is embedded in the note. Accordingly, this antenna is a closed dipole. The loop can also be said to form the secondary winding of an air-core transformer having its primary winding placed within the authentication apparatus. This is similar to the arrangement provided for contact-less smart cards.

[0027] Whereas the absence of contacts is a definite advantage with smart cards, this may not always be so in the instance of banknotes. In fact, the availability of at least two contacts on the banknote, for communicating with and powering the integrated circuit IC, allows the layout of the latter to be simplified and its cost reduced, which constitutes a critical factor in an application such as this. Furthermore, the occasions when a banknote is to be positively authenticated are far less frequent than in the operation of a smart card, and therefore, the inconvenience represented by the electric contact is less of a penalty.

[0028] For the purpose, the banknote BN may additionally include two electric conductors C1 and C2 connected electrically to the terminals T1 and T2, and having two external contact pads A1 and A2, respec-

tively. These pads may be on the same face or different faces of the banknote BN, and in the extreme, located at an edge thereof.

[0029] Alternatively, the terminals T1 and T2 of the integrated circuit IC could be made accessible directly from outside the banknote BN for electric contacting, as in the embodiment of Figure 9. The terminals might locate on and be accessed from different sides of the banknote BN.

[0030] In either of these cases where the banknote BN is provided with external contact pads, the integrated circuit IC layout can be similar to that of a smart card "with contacts".

[0031] The electric conductors C1, C2, LP can be formed in the banknote by any of several methods: they may be printed in conductive ink, be thin wires embedded in the note, or be very thin (e.g. 300Å thick) metal strips deposited onto thin (e.g. 10µm thick) plastics strips embedded in the note.

[0032] Among the most critical factors to a large-scale implementation of this invention are the cost of the integrated circuit, more generally of the banknote, and the thickness dimension of the integrated circuit.

[0033] The cost of the security device, i.e. the integrated circuit, ought to be related to the denomination of the note (banknote, check, bill, bond, etc.). For example, the cost of a fairly simple integrated circuit may amount to a half-dollar and, accordingly, it would seem reasonable to use the circuit for denominations upward of fifty dollars. Therefore, if the utilization of this invention is to be extended to include lower denominations, of primary consideration become: the use of inexpensive semiconductor manufacturing processes; an integrated circuit layout of small area, and hence simple circuitry, so that a semiconductor wafer can accommodate a large number of them; and the adoption of very large volume manufacturing methods.

[0034] For the banknote to be easy to handle, the thickness of the insert consisting of the integrated circuit should not exceed that of standard banknote paper. To quote, standard sheet paper for office use is 30 to 60µm thick, ply paper for banknote printing has a thickness of 50 to 100µm, thin opaque or transparent sheet plastics may range in thickness from 8 to 15µm, and the thickness of an integrated circuit for smart cards is approximately 180µm.

[0035] Thus, a suitable thickness for the integrated circuit in this invention would be less than 100µm, preferably less than 50µm. For example, using the CMP (Chemical Mechanical Polishing) method, the thickness of the silicon die has been cut down to 40µm in the lab, without damaging any of the circuitry included in the integrated circuits that form the chip.

[0036] Some embodiments of a banknote according to the invention will now be described with the aid of sectional views thereof. These sectional views are taken at the locations of the integrated circuit IC, and of the conductors C1, C2, LP, where provided. The banknote con-

struction obviously is simpler elsewhere.

[0037] In Figure 4, the banknote comprises a first sheet paper layer L1 and a second sheet paper layer L2 overlying the first. Sandwiched between these layers is the integrated circuit IC provided with (visible) T1 and (invisible) T2 terminals. Also sandwiched between the layers L1 and L2 are a thin plastics layer L3 and a very thin metal layer, deposited over the layer L3 that forms the conductor C1. The conductor C1 has a contact pad A1 which appears at the surface of the layer L2 and contacts the terminal T1.

[0038] In Figure 5, the banknote comprises first L1 and second L2 overlapping sheet paper layers, and first L3 and second L4 thin plastics layers which are apertured at the integrated circuit IC. A very thin metal layer is deposited onto the layer L3 and forms the conductor C2. The integrated circuit IC is sandwiched between the layers L3 and L4 and has (invisible) T1 and (visible) T2 terminals. Figure 5 could be, for example, a cross-section through the banknote BN of Figure 1.

[0039] In Figure 6, the banknote comprises first L3 and second L4 thin overlapping plastics layers, and first L1 and second L2 overlapping sheet paper layers. The layers L1 and L2 overlie the layers L3 and L4. The layers L1 and L2 are apertured at the integrated circuit IC. The integrated circuit IC is sandwiched between the layers L3 and L4, and provided with an integrated antenna ANT. Figure 6 could be, for example, a cross-section through the banknote BN of Figure 3.

[0040] In Figure 7, the banknote comprises first L1 and second L2 overlapping sheet paper layers, and a thin plastics layer L4 placed between the layers L1 and L2. The layer L2 is apertured at the integrated circuit IC. The integrated circuit IC is placed between the layers L1 and L4 and provided with (visible) T1 and (invisible) T2 terminals. Printed in conductive ink onto the layer L1 is a loop LP in contact with the terminals T1 and T2. Figure 7 could be, for example, a cross-section through the banknote BN of Figure 2.

[0041] In Figure 8, the banknote comprises a single sheet paper layer LL, and first L3 and second L4 thin plastics layers enclosing it. The layer LL is apertured at the integrated circuit IC. The integrated circuit IC is placed between the layers L3 and L4 and provided with an integrated antenna ANT. Figure 8 could be, for example, a cross-section through the banknote BN of Figure 3.

[0042] In Figure 10, the banknote comprises a single sheet paper layer LL, and first L3 and second L4 thin plastics layers enclosing it. The layer LL is apertured at the integrated circuit IC. The integrated circuit IC is placed between the layers L3 and L4 and provided with two terminals T1 and T2 which appear at the surface of the layer L4 and, therefore, can be accessed directly from outside the banknote BN for electric contact purposes. Figure 10 is a cross-section through the banknote BN of Figure 9.

[0043] In all of the above embodiments, the integrated

circuit IC is fully isolated from the note exterior. In general, the integrated circuit IC should be provided with suitable passivation layers to protect and seal it at least from moisture.

[0044] As previously mentioned, the information that can be stored in the integrated circuit IC is, for example, a real or par value, the identity, the issuer, and the date of issuance of the note.

[0045] The integrated circuit IC may be adapted to store this and/or other elements of information in a crypted form, such as read and/or write passwords.

[0046] Thus, the authentication operation corresponds to reading the information from the integrated circuit and checking it for correctness in an automatic or manual manner. The reading may be free or subordinate to the integrated circuit receiving a read password.

[0047] Of course, such information has been preliminarily recorded in the integrated circuit. This can be done either by the manufacturer of the integrated circuit or the issuer or a distributor acting on behalf of the issuer (e.g., a bank branch office). The recording of information could be effected, if desired, by a number of entities at different stages; each entity would typically enter information of its own province.

[0048] In view of the low-cost fabrication of integrated circuits at tyro level being virtually impossible, forgers may be expected to attempt the removal of integrated circuits from low denomination notes, altering the information stored therein, and transferring them to forged notes of higher denomination.

[0049] To prevent forgers from tampering with stored information, it can be arranged for the integrated circuit to request a password before information can be written thereinto.

[0050] In a simpler way, the integrated circuit may be provided with a non-volatile memory which can be programmed only once, that is by an irreversible physical action.

[0051] Such a memory could be selected from ROMs, PROMs, UPROMs or CAMs or fused memories, EPROMs without erase windows or EEPROMs without erase circuits, in decreasing order of security level. Another factor not to be overlooked is ease of programming. ROMs can only be factory programmed (so that each note must be provided with an individually different integrated circuit), while PROMs and EPROMs require high program voltages. The manufacturing cost of the integrated circuit is also a factor.

[0052] An alternative choice would be to provide the integrated circuit with a non-volatile memory for storing identity information, and with a security circuit having a non-erasable (i.e. programmable only once) memory, such as a fused memory, and being effective to inhibit programming of the non-volatile memory in relation to the contents of the non-erasable memory. In this case, the following procedure may be used. Each time that the integrated circuit receives a program command, it checks the non-erasable memory for its contents: if

these contents reveal that the non-volatile memory has already been programmed, the program command is not executed; otherwise, the command is executed, and the contents of the non-erasable memory are set to prevent future re-programming. This safeguard against re-programming may be provided for segments rather than the whole memory.

**[0053]** To avoid interference on the stored information, and physical attack (by radiation or thermal treatment), it should not be overlooked the possibilities offered by electrically re-programming, e.g. bits not yet programmed within an already programmed byte. A way of solving this problem systematically is to have the information to be stored suitably encoded. For example, by arranging for two bits, to be stored by the code "zero" -> "01" and "one" -> "10", to correspond to each information bit, it would become impossible to turn a "zero" into a "one", or a "one" into a "zero", by any operations attempted on the memory after the initial programming operation.

**[0054]** A second non-volatile memory, with reduced or no protection, could be provided additionally to a fully safeguarded non-volatile memory, e.g. for bank branch offices to record information in a banknote. For example, the first memory might be of the fused type and the second memory be either safeguarded by means of a write password or be freely programmable.

**[0055]** This can also be achieved with a single memory array divided into two or more segments. For example, the non-erasable memory may be adapted to store a plurality of bits, each bit being associated with a different memory segment, and some of these bits having fixed informational contents to indicate that the segment is freely programmable, while other bits would have varying informational contents as previously explained.

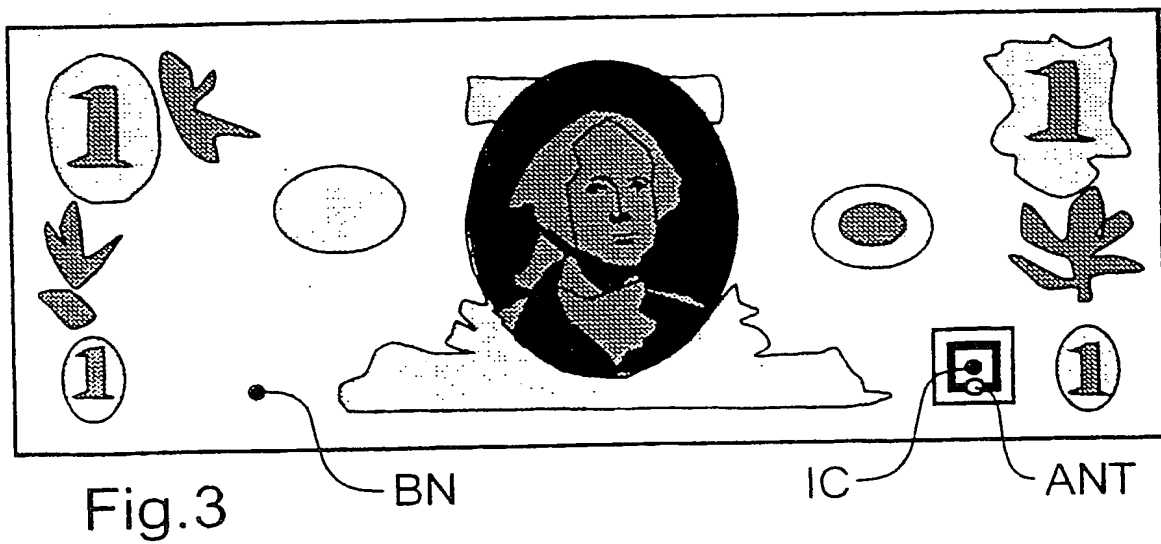
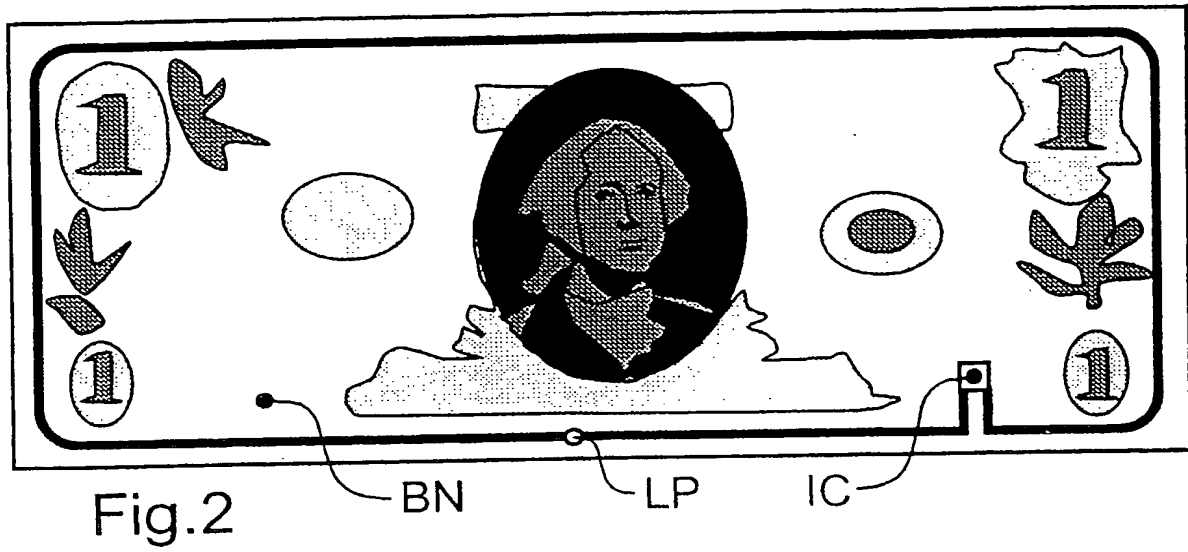
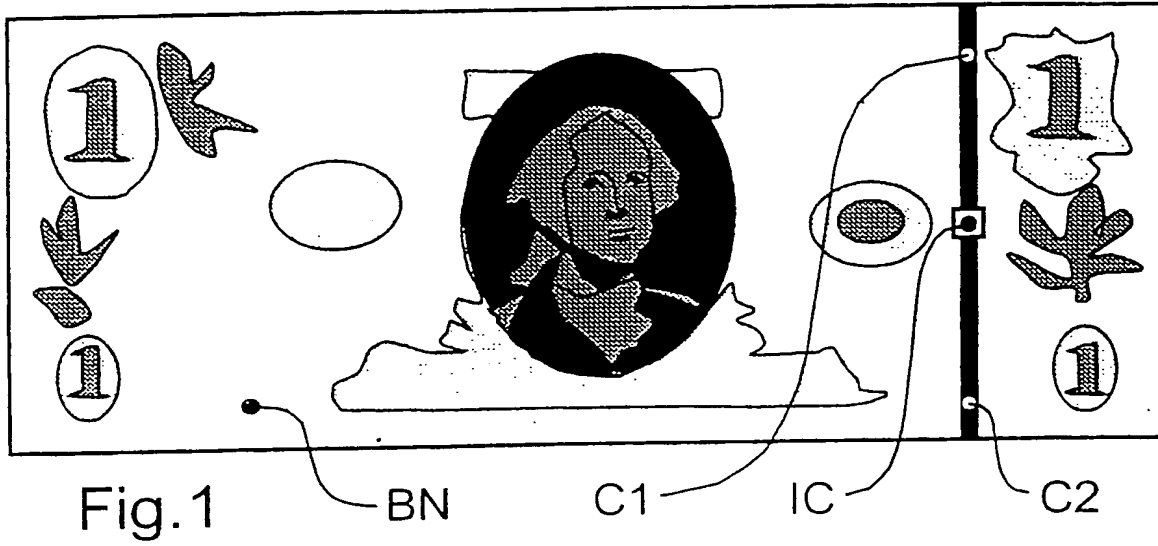
**[0056]** Of course, all of the technological and economical considerations submitted hereinabove would be subject to continual evolution.

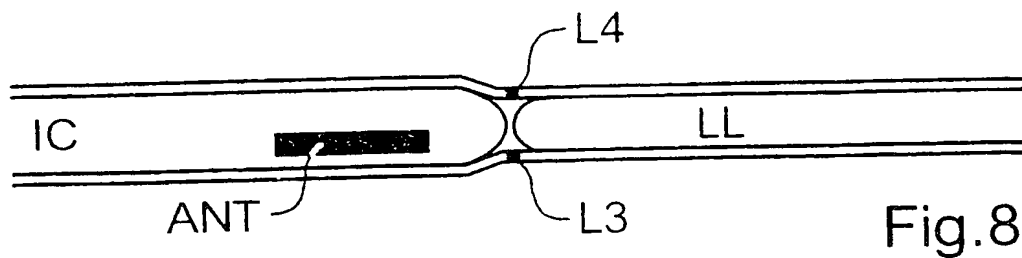
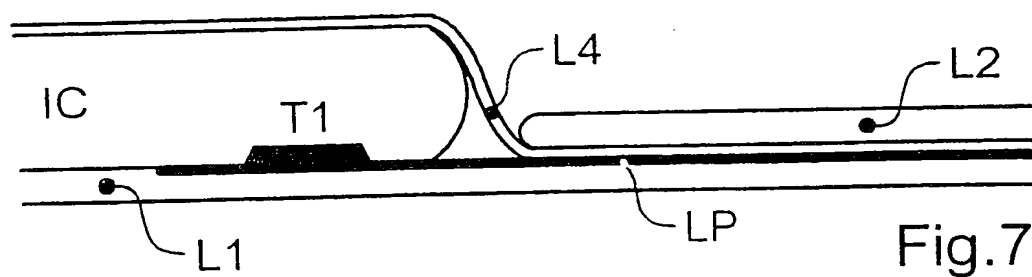
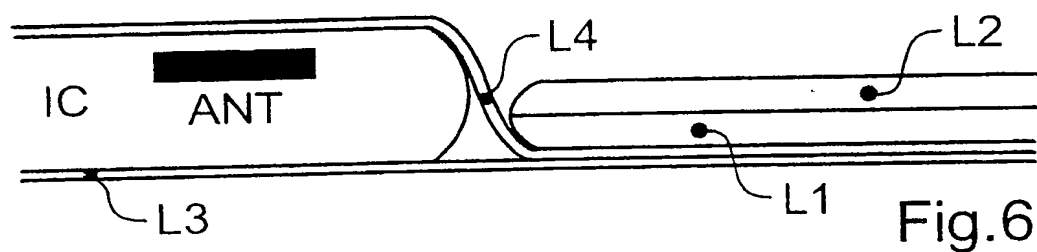
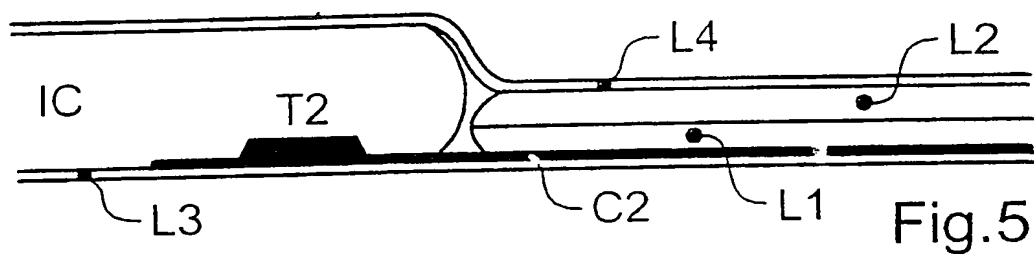
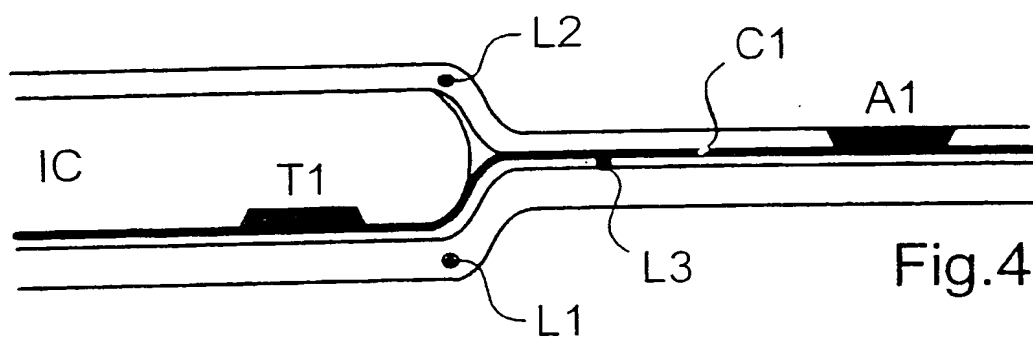
#### Claims

1. A currency note (BN), characterized in that it includes at least one integrated circuit (IC) as its identification and/or authentication element.
2. A note (BN) according to Claim 1, wherein the integrated circuit (IC) has an integrated antenna (ANT) and no terminals.
3. A note (BN) according to Claim 1, wherein the integrated circuit (IC) has two or more terminals (T1,T2).
4. A note (BN) according to Claim 1, wherein the integrated circuit (IC) thickness is less than 100µm, preferably less than 50µm.
5. A note (BN) according to Claim 3, further including

an antenna (C1,C2;LP) which is connected electrically to said terminals (T1,T2).

6. A note (BN) according to Claim 5, wherein the antenna comprises two electric conductors (C1,C2) embedded in the note.
7. A note (BN) according to Claim 5, wherein the antenna consists of a loop (LP) comprising an electric conductor embedded in the note.
8. A note (BN) according to Claim 3, further including two electric conductors (C1,C2) connected electrically to said terminals and provided with two external contact pads (A1,A2), respectively.
9. A note (BN) according to Claim 3, wherein said terminals (T1,T2) are accessible directly from outside the note for electric contacting purposes.
10. A note (BN) according to Claim 1, wherein the integrated circuit (IC) is adapted to store information.
11. A note (BN) according to Claim 10, wherein the integrated circuit (IC) is adapted to store information relating to the face value of the note.
12. A note (BN) according to Claim 10, wherein the integrated circuit (IC) is adapted to store information relating to the identity of the note.
13. A note (BN) according to Claim 10, wherein the integrated circuit (IC) is adapted to store information relating to the issuer of the note.
14. A note (BN) according to Claim 10, wherein the integrated circuit (IC) is adapted to store information relating to the date of issuance of the note.
15. A note (BN) according to Claim 10, wherein the integrated circuit (IC) is adapted to store different elements of information at different times.
16. A note (BN) according to Claim 10, wherein the integrated circuit (IC) includes a non-volatile memory programmable only once.
17. A note (BN) according to Claim 10, wherein the integrated circuit (IC) includes a non-volatile memory for storing said information, as well a security circuit provided with a non-erasable memory and adapted to inhibit the programming of said non-volatile memory in relation to the informational contents of said non-erasable memory.





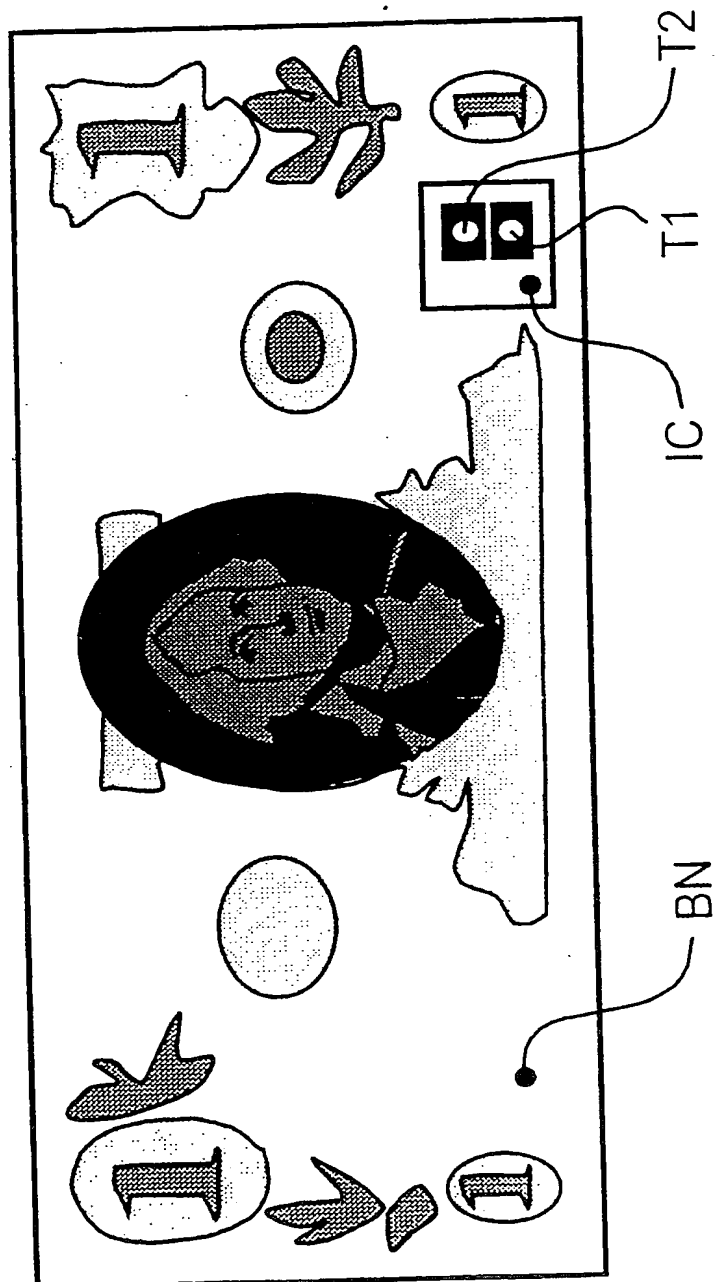


Fig. 9

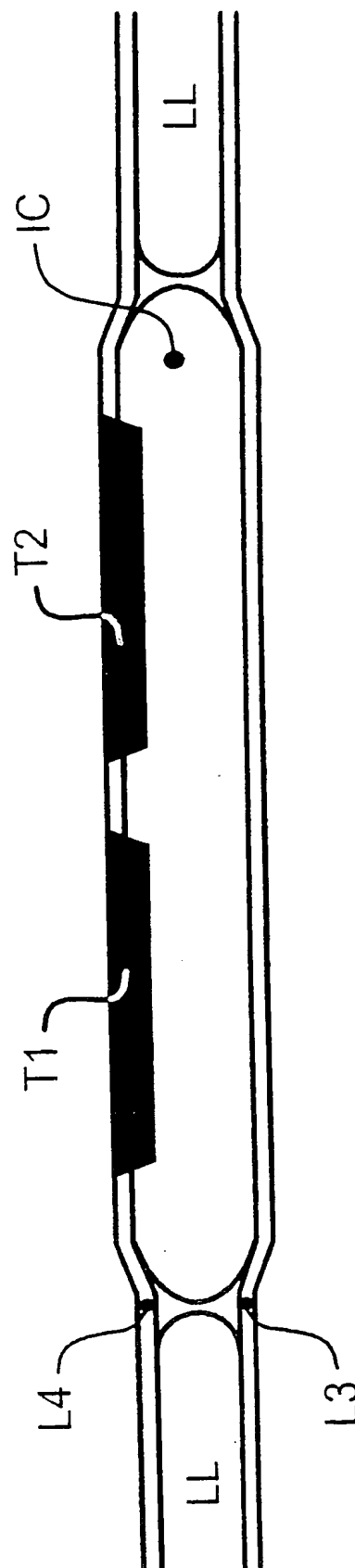


Fig. 10





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# EUROPEAN SEARCH REPORT

Application Number  
EP 97 83 0464

| DOCUMENTS CONSIDERED TO BE RELEVANT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                    |                                                   |                                              |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|----------------------------------------------|
| Category                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Citation of document with indication, where appropriate, of relevant passages                                                      | Relevant to claim                                 | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
| X<br>A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | EP 0 019 191 A (BBC BROWN BOVERI & CIE)<br>* claim 1: figure 1 *                                                                   | 1<br>2-17                                         | G07D7/00                                     |
| X<br>A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | "CURRENCY WITH AN INTEGRATED CHIP"<br>IBM TECHNICAL DISCLOSURE BULLETIN,<br>vol. 32, no. 5A, October 1989,<br>page 427 XP000048976 | 1<br>2-17                                         |                                              |
| A                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | US 4 472 627 A (WEINBERGER LESTER)<br>* claim 1: figure 1 *                                                                        | 1-17                                              |                                              |
| A,D                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | US 5 566 441 A (MARSH MICHAEL J C ET AL)<br>* claim 1: figure 1 *                                                                  | 1-17                                              |                                              |
| A,D                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | US 5 537 105 A (MARSH MICHAEL J C ET AL)<br>* claim 1: figure 1 *                                                                  | 1-17                                              |                                              |
| The present search report has been drawn up for all claims                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                    |                                                   |                                              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                    |                                                   |                                              |
| Place of search<br>THE HAGUE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                    | Date of completion of the search<br>21 April 1998 | Examiner<br>Kirsten, K                       |
| <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone<br/>Y : particularly relevant if combined with another document of the same category<br/>A : technological background<br/>O : non-written disclosure<br/>P : intermediate document</p> <p>T : theory or principle underlying the invention<br/>E : earlier patent document, but published on, or after the filing date<br/>D : document cited in the application<br/>L : document cited for other reasons<br/>3 : member of the same patent family, corresponding document</p> |                                                                                                                                    |                                                   |                                              |

1 PO FORM 1503 03/82 (P04C01)